Amendments to the Drawings:

The attached replacement sheet of drawing includes changes to FIG. 3 to show a "check value" as recited in the claims.

Attachments following last page of this Amendment:

Replacement Sheet (1 page)
Annotated Sheet Showing Change (1 page)

REMARKS

Claims 1-8 are pending in this application, of which claims 1 and 4 are independent. Favorable reconsideration and further examination is respectfully requested in view of the foregoing amendments and following remarks.

Applicants have addressed the Examiner's objection to the title. In particular, Applicants have amended the title to be consistent with that of the parent application, U.S. serial no. 09/378,643. Applicants have also enclosed a replacement drawing sheet to show a "check value" as recited in the claims.

The claims were objected to for informalities. Applicants have made appropriate amendments and respectfully request withdrawal of the objections.

Examiner Interview of April 19, 2006

Applicants thank the Examiner for the helpful and courteous phone interview with Applicants' representatives, Mr. Occhiuti and Mr. Su. Without conceding any arguments, Applicants appreciate the Examiner's clarification of his interpretation of the claim limitations in view of the references.

Double Patenting Rejection

Claims 1-6 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-6 of commonly owned U.S. patent no. 6,629,199. Applicants have enclosed a terminal disclaimer in compliance with 37 CFR 1.321(c) and respectfully request withdrawal of the rejection.

35 USC 103(a) Rejections

Claim 1

Independent claim 1 was rejected under 35 USC 103(a) over Yeger et al. (U.S. patent no. 5,809,435) or Vishlitzky (U.S. patent no. 6,029,229) in view of Fukuda et al. (U.S. patent no. 4,698,810) or Sze (U.S. patent no. 6,092,231).

Applicants submit that there is no motivation to combine Yeger or Vishlitzky with Fukuda or Sze to teach a digital data storage system including "a memory configured to store, associated with each storage location, a descriptor of data, the descriptor of data comprising a check value for the record stored in the respective location associated with the descriptor of data," as recited in amended claim 1.

Specifically, Yeger discloses a digital data processing system with a plurality of track descriptors, each track descriptor

> includes information for the associated track of the storage device 22, including whether a copy of the data stored on the track is cached in the cache memory 31, and, if so, the identification of the cache slot 35(s) in which the data is cached. In particular, each track descriptor 43(c)(t) includes a cached flag 44(c)(t) and a cache slot pointer 45(s)(t). The cached flag 44(c)(t), if set, indicates that the data on the track associated with the track is cached in a cache slot 35(s), and the cache slot pointer 45(s)(t) identifies the particular cache slot in which the data is cached. In addition, each track descriptor 43(c)(t) includes a used flag 46(c)(t) which may be used to indicate whether the data, after being stored in the cache slot identified by the cache slot pointer 43(c)(t), has been used by the host computer 11(n)(k) during a retrieval operation.

(col. 7, lines 39-60). Yeger teaches a track descriptor including a cached flag, a cache slot pointer, and a used flag, but makes no mention of the possibility of or desire for error correction, error checking, or using a check value to verify that data is from a particular track of the storage device.

Vishlitzky discloses a digital data storage system with a plurality of track descriptors, each track descriptor

> includes a general track information section 40 and a record specific information section 41. The general track information section 40 includes information about the track, including such information as whether the track is cached in the cache memory 31 and, if so, a pointer to the cache slot 31(s) in which the track is cached. In addition, the general track information section 40 indicates the number of records in the track, and provides some supplemental formatting information for the records in the track. The record specific information section 41, on the other hand, contains record-specific basic formatting information for the respective records in the track.

(col. 9, lines 1-13). Vishlitzky teaches a track descriptor including a general track information section and a record specific information section containing formatting information for the records in the track. However, Vishlitzky makes no mention of the possibility or desire to use either information section for error correction, error checking, or with check values to verify that data is from a particular track of the storage device.

Therefore, there is no motivation to combine either Yeger or Vishlitzky with Fukuda or Sze to teach a "descriptor of data comprising a check value for the record stored in the respective location associated with the descriptor of data," as recited in amended claim 1.

Accordingly, Applicants submit that the rejection is a hindsight reconstruction, using Applicants' claim as a template to reconstruct the invention by picking and choosing isolated disclosures from the prior art. This is impermissible under the law. For example, in *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992), the Federal Circuit stated:

> It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). This court has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (quoting *In re Fine*, 837 F.2d at 1075, 5 USPQ2d at 1600)

The present rejection fits the court's description of what may not be done under section 103. The Examiner has merely listed certain components of Applicants' claim and then located isolated disclosures of those components. The law requires more than that.

The Examiner must show where the prior art provides a motivation to combine the references he/she has combined in the obviousness rejection. Absent a motivation to combine, obviousness has not been demonstrated. As the Federal Circuit stated in *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934, 15 USPQ2d 1321, 1323 (Fed. Cir. 1990), it is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor.

There is a further reason why independent claim 1 is patentably distinct from the references cited by the Examiner. The Examiner acknowledges that neither Yeger nor Vishlitzky specifically discloses the descriptor having a check value for the record stored in the respective storage location associated with the descriptor (see page 7, Office Action). However, the Examiner argues that both Fukuda and Sze disclose this feature and that it would have been obvious to a person of ordinary skill in the art to modify either Yeger or Vishlitzky to include such a feature. Applicants disagree. In particular, even if there was motivation to combine either Yeger or Vishlitzky with Fukuda or Sze, a person of ordinary skill in the art still would not arrive at the invention recited in claim 1.

Fukuda discloses an optical disk system using a cyclic redundancy check (CRC) code in conjunction with an error correction code (ECC) to detect that the read circuit has performed the error correcting operation erroneously on the error which is beyond the error correcting capability of the read circuit (col. 4, lines 23-28). The Examiner interprets the CRC code or the ECC code to be a "check value" as recited in the claims. Even if this were true, which Applicants do not concede, Fukuda does not disclose or render obvious a "descriptor of data comprising a check value for the record stored in the respective location associated with the descriptor of data," as recited in amended claim 1.

In this regard, Fukuda teaches that "each of the data blocks is divided into a plurality of code words each of which has added thereto an error correcting code" (col. 2, lines 17-19), and the "data of each code word and error correcting code are interleaved" (col. 2, lines 32-33). The Fukuda system stores the error correcting code together with the data, and thus, increases the amount of information that needs to be stored on a storage device. Applicants' descriptor of data system provides a distinct advantage over Fukuda by reducing the amount of information about the data which would otherwise need to be stored on the storage device.

Sze discloses a circuit and method for using cyclic redundancy check (CRC) to improve the accuracy and speed of error detection and correction when reading bytes from a disk in a disk drive (col. 2, lines 10-13). The Examiner interprets the CRC code to be a "check value" as recited in the claims. Even if this were true, which Applicants do not concede, Sze does not

disclose or render obvious a "descriptor of data comprising a check value for the record stored in the respective location associated with the descriptor of data," as recited in amended claim 1.

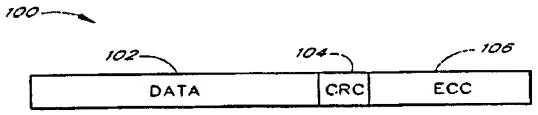

FIG. 1

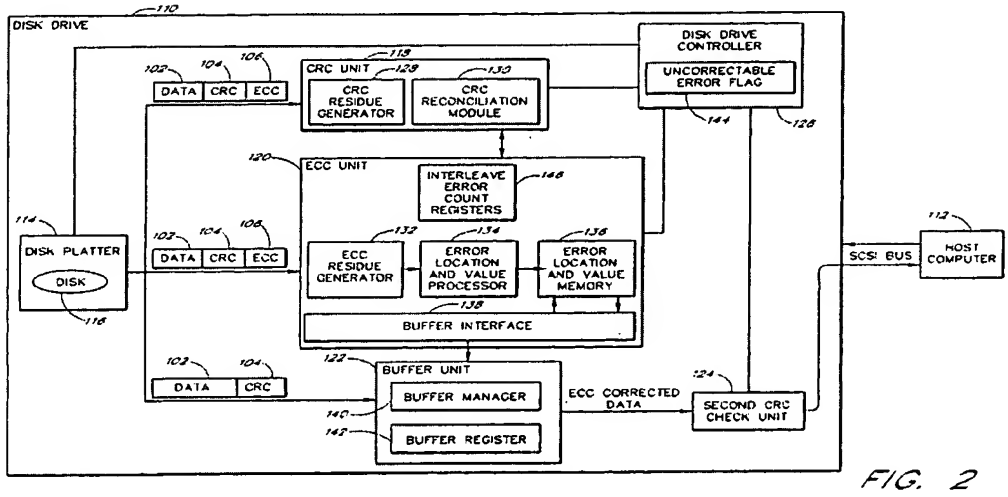

FIG. 2

In reference to the above figures, the "CRC and the ECC bytes are appended to the end of the set of data bytes. The data bytes, CRC bytes and ECC bytes together make up a 'sector'" (col. 1, lines 21-23). FIG. 1 illustrates a sector 100 of bytes with a CRC portion 104 and ECC portion 106. The Sze system stores the error correcting code together with the data, and thus, increases the amount of information that needs to be stored on a storage device. Applicants' descriptor of data system provides a distinct advantage over Sze by reducing the amount of information about the data which would otherwise need to be stored on the storage device.

Moreover, Figure 2, reference 144 does not disclose or suggest a descriptor of data having a check value. In this regard, Sze teaches that reference 144 is an "uncorrectable error flag" which is "set" when the ECC unit 120 detects an uncorrectable error in the data 102 (col. 7,

lines 43-44). While the uncorrectable error flag 144 may describe the data, it does not include a check value as recited in claim 1.

Therefore, neither Fukuda nor Sze discloses or renders obvious a "descriptor of data comprising a check value for the record stored in the respective location associated with the descriptor of data," as recited in amended claim 1.

For at least these reasons, claim 1 is patentable over Yeger, Vishlitzky, Fukuda or Sze, either individually or in combination. Applicants further submit that because claims 2, 3, and 7 depend from claim 1, these dependent claims are patentable for at least the same reasons that claim 1 is patentable.

Claim 4

Independent claim 4 was rejected under 35 USC 103(a) over Yeger or Vishlitzky in view of Fukuda or Sze. For reasons discussed above in conjunction with claim 1, Applicants submit that there is no motivation to combine Yeger or Vishlitzky with Fukuda or Sze to teach a method of operating a digital data storage system including using "a memory configured to store, associated with each storage location, a descriptor of data, the descriptor of data comprising a check value for the record stored in the respective storage location associated with the descriptor of data," as recited in amended claim 4. Moreover, even if there was motivation to combine either Yeger or Vishlitzky with Fukuda or Sze, a person of ordinary skill in the art still would not arrive at the invention recited in claim 4. For at least these reasons, claim 4 is patentable over Yeger, Vishhlitzky, Fukuda or Sze, either individually or in combination. Applicants further submit that because claims 5, 6, and 8 depend from claim 4, these dependent claims are patentable for at least the same reasons that claim 4 is patentable.

It is believed that all of the pending claims have been addressed. The absence, however, of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been addressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this

paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: May 1 2006

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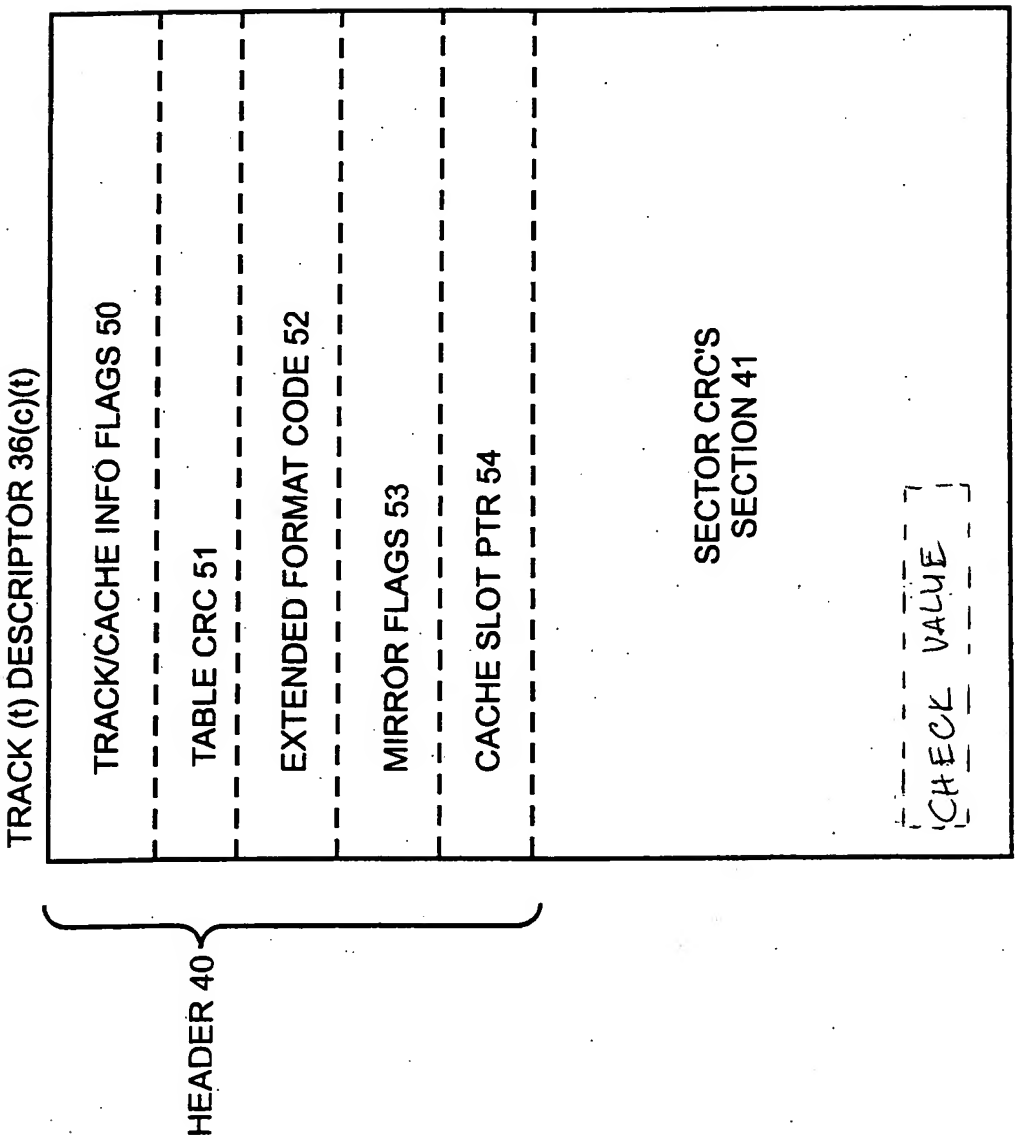
TRACK (t) DESCRIPTOR 36(c)(t)
TRACK/CACHE INFO FLAGS 50
TABLE CRC 51
EXTENDED FORMAT CODE 52
MIRROR FLAGS 53
CACHE SLOT PTR 54
SECTOR CRC'S SECTION 41
CHECK VALUE
HEADER 40

FIG. 3